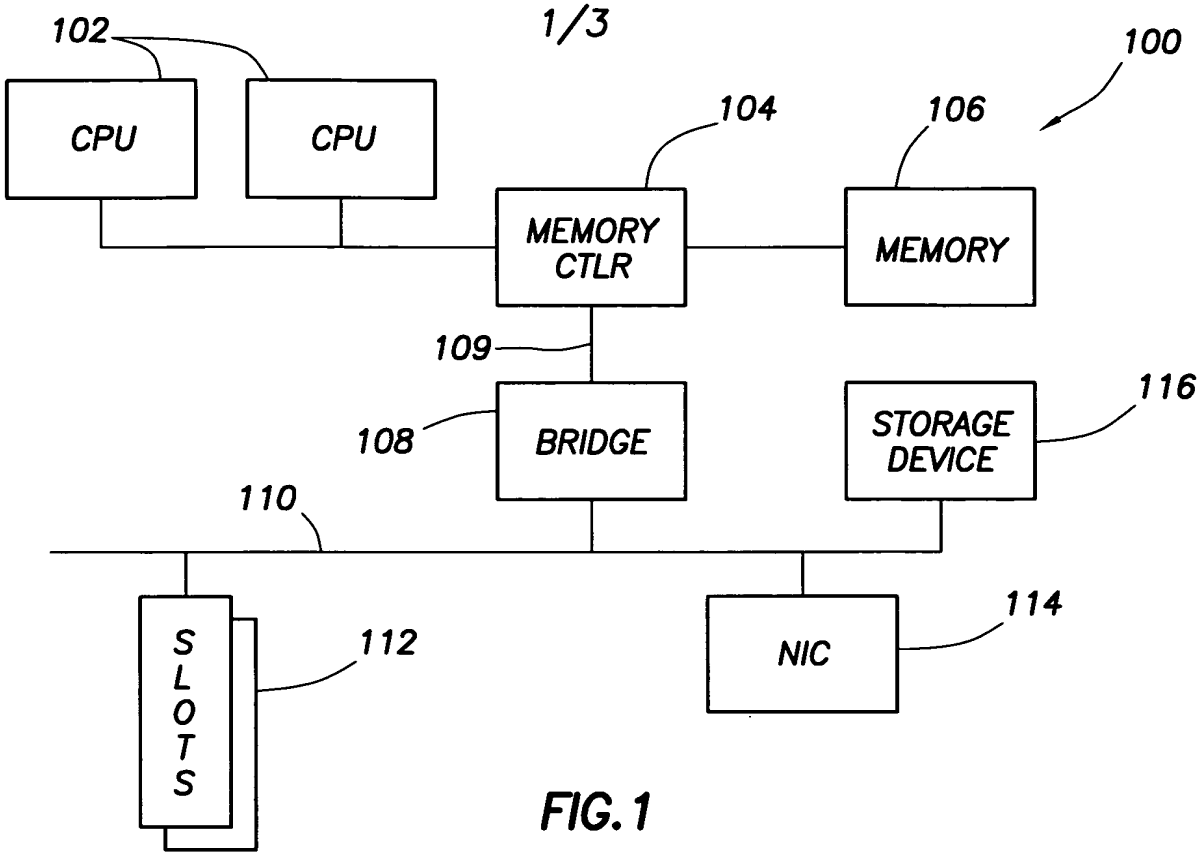
102
CPU
CPU
104
106
100
MEMORY CTLR
MEMORY
109
108
BRIDGE
STORAGE DEVICE
116
110
S L O T S
112
NIC
114

FIG. 1

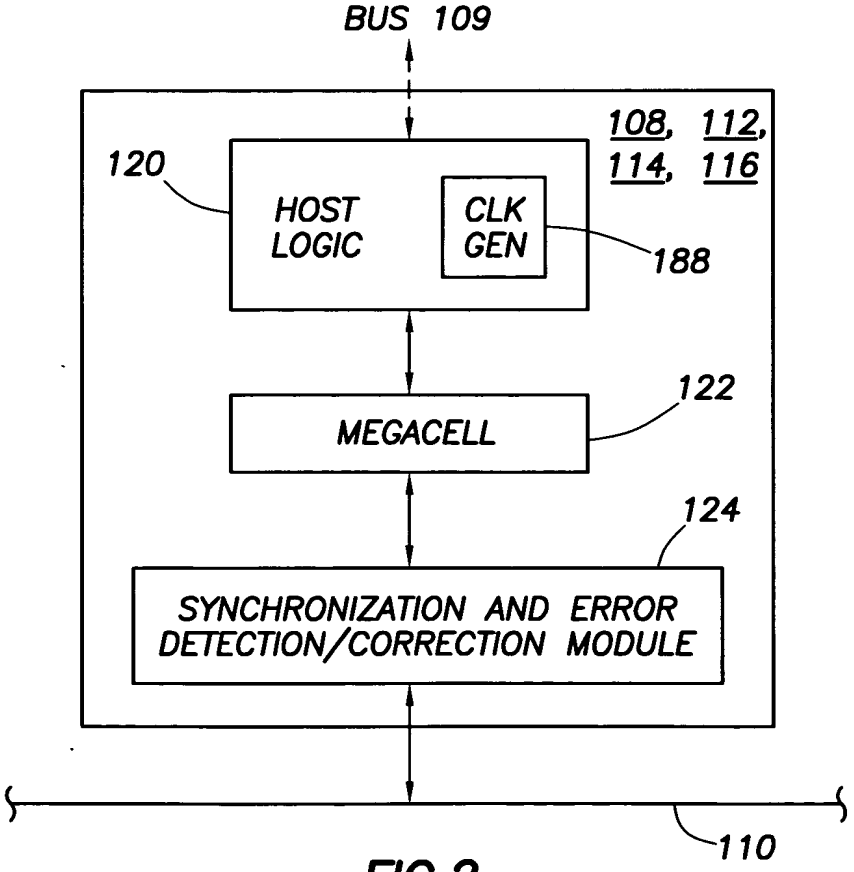
BUS 109
108, 112, 114, 116
120
HOST LOGIC
CLK GEN
188
122
MEGACELL
124
SYNCHRONIZATION AND ERROR DETECTION/CORRECTION MODULE
110

FIG. 2

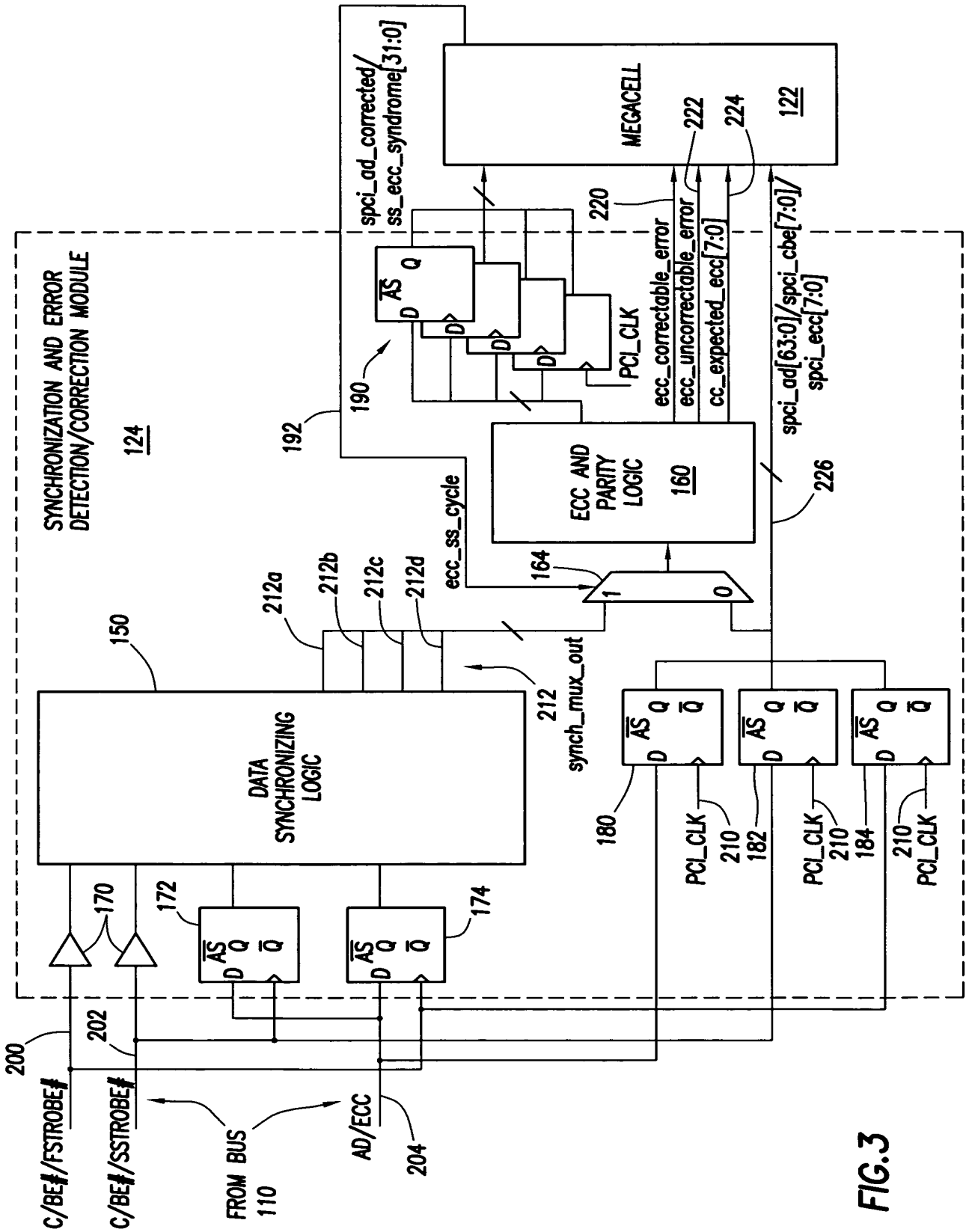
SYNCHRONIZATION AND ERROR DETECTION/CORRECTION MODULE
124
MEGACELL
122
spci_ad_corrected/ ss_ecc_syndrome[31:0]
ECC AND PARITY LOGIC
160
DATA SYNCHRONIZING LOGIC
150
PCI_CLK
ecc_correctable_error
ecc_uncorrectable_error
cc_expected_ecc[7:0]
spci_ad[63:0]/spci_cbe[7:0]/ spci_ecc[7:0]
ecc_ss_cycle
synch_mux_out
C/BE#/FSTROBE#
C/BE#/SSTROBE#
FROM BUS 110
AD/ECC
200
202
204
170
172
174
180
182
184
190
192
210
212
212a
212b
212c
212d
220
222
224
226

FIG.3

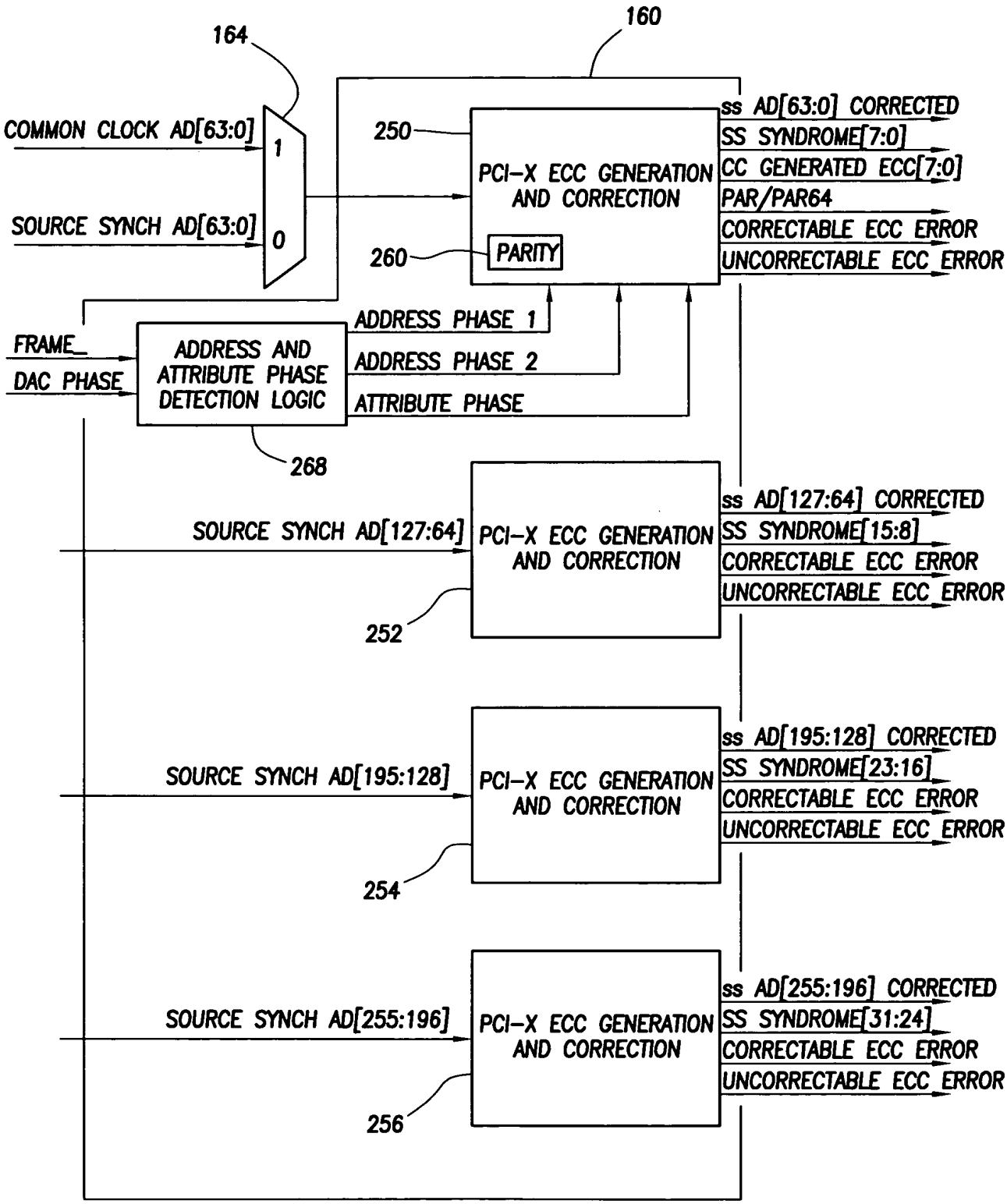
164
160
COMMON CLOCK AD[63:0]
SOURCE SYNCH AD[63:0]
1
0
250
PCI-X ECC GENERATION AND CORRECTION
260
PARITY
ss AD[63:0] CORRECTED
SS SYNDROME[7:0]
CC GENERATED ECC[7:0]
PAR/PAR64
CORRECTABLE ECC ERROR
UNCORRECTABLE ECC ERROR
FRAME
DAC PHASE
ADDRESS AND ATTRIBUTE PHASE DETECTION LOGIC
ADDRESS PHASE 1
ADDRESS PHASE 2
ATTRIBUTE PHASE
268
SOURCE SYNCH AD[127:64]
PCI-X ECC GENERATION AND CORRECTION
252
ss AD[127:64] CORRECTED
SS SYNDROME[15:8]
CORRECTABLE ECC ERROR
UNCORRECTABLE ECC ERROR
SOURCE SYNCH AD[195:128]
PCI-X ECC GENERATION AND CORRECTION
254
ss AD[195:128] CORRECTED
SS SYNDROME[23:16]
CORRECTABLE ECC ERROR
UNCORRECTABLE ECC ERROR
SOURCE SYNCH AD[255:196]
PCI-X ECC GENERATION AND CORRECTION
256
ss AD[255:196] CORRECTED
SS SYNDROME[31:24]
CORRECTABLE ECC ERROR
UNCORRECTABLE ECC ERROR

FIG.4